IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Tremblay, Marc		
Assignee:	Sun Microsystems, Inc.		
Title:	A Grouping Logic Circuit In A Pipelined Superscalar Processor		
Serial No.:	Unassigned	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	SP-1391-1D US		

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San Jose, California
July 25, 2000

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COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

IN THE CLAIMS

Please amend Claim 1 as follows:

1. (Amendment) A central processing unit, comprising:

a plurality of functional units, each functional unit adapted to execute an instruction of said central processing unit; and

a grouping logic circuit, including a number of pipeline stages and receiving, at each processor cycle, a group of instructions and one or more state vectors each representing states of instructions previously received at said grouping logic circuit in a preceding processor cycle wherein, based on said state vectors, said grouping logic circuit [dispatching] dispatches each of said currently received instructions to be

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979